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NITRIDE ETCHSTOP FILM TO PROTECT METAL-INSULATOR-METAL CAPACITOR DIELECTRIC FROM DEGRADATION AND METHOD FOR MAKING SAME

Cross Reference to Related Applications

This application is based on Provisional Application Number 60/354,882, filed on February 5, 2002.

Background of the Invention

[0001] Field of the Invention

[0002] The present invention generally relates to a metal-insulator-metal (MIM) capacitor in a semiconductor device and a method of fabricating the same. More particularly, this invention relates to the use of a nitride etchstop layer to prevent degradation of the dielectric of the MIM capacitor.

[0003] Description of the Related Art

[0004] In a multilayer semiconductor, when vias are formed to contact the metal plates of an MIM capacitor, greater control of forming the vias and maintaining a shape of the via are obtained by using an anisotropic etch process, such as, reactive ion etching (RIE), as opposed to an isotropic etching process, such as, a wet chemical etch. RIE is particularly useful for forming vias when the depth and corresponding aspect ratio of the via are relatively large. However, forming vias that contact the capacitor plates of an MIM capacitor by RIE and other anisotropic etch processes, which use ions and/or plasma, can produce degradation of the capacitor dielectric and even plate-to-plate

electrical shorting of the MIM capacitor.

[0005] Dielectric breakdown is caused by excessive electrical charge build-up across the plates, which may result from an aggressive RIE etch that lands a via on the top plate of the MIM capacitor or other anisotropic etch processes that are performed at levels above the MIM capacitor. Dielectric breakdown results from permanent conductive channels being formed in the dielectric, which degrade the insulative properties of the dielectric.

[0006] Plate-to-plate electrical shorting of the MIM capacitor results from either top plate etch-through by an aggressive RIE etch that lands on the top plate or by dielectric breakdown caused by aggressive anisotropic etching above the MIM capacitor that causes electrical shorting across the dielectric layer.

[0007] Degradation of long term reliability of the dielectric layer of the MIM capacitor is measured by time dependent dielectric breakdown, where the time to breakdown is measured under a constant electric field of about 6-9MV/cm. The conventionally fabricated MIM capacitor dielectric layer often shows degradation of long term reliability, when compared to the expected lifetime of a comparable defect-free dielectric layer.

[0008] During conventional fabrication of a multilayer semiconductor device including an MIM capacitor, RIE etch processes that cause dielectric degradation include: RIE patterning of the top plate of the MIM capacitor, that is, the Q etch; RIE via etch processes that create vias that land on the top and/or bottom plates of the MIM capacitor; and other anisotropic etch processes that take place above the MIM capacitor subsequent to completion of the MIM capacitor processing, such as, pattern etching of a wiring level in electrical contact with the top and/or bottom plates.

[0009] Via formation by RIE requires overetch in order to ensure proper landing of the via on both the top and bottom plate. This overetch exposes the top and bottom capacitor plates to a longer duration and a greater magnitude of electrical charge and ion/plasma damage, associated with the RIE. However, since the top plate is landed on first, the top plate experiences greater electrical charging and more ion/plasma damage from the effects of this overetch.

Brief Summary of the Invention

[0010] In view of the foregoing and other problems and disadvantages of conventional methods, an advantage of the present invention is the extended lifetime of an MIM capacitor dielectric within a multilayer semiconductor device that may be attained by depositing a nitride etchstop layer above the MIM capacitor to prevent degradation of the capacitor dielectric, which may be caused by excessive electrical charging and ion/plasma damage of the plates of the MIM capacitor by anisotropic etch processes.

[0011] Another advantage of the present invention is preventing plate-to-plate electrical shorting of the MIM capacitor within a multilayer semiconductor device, which may be caused by either top plate etch-through or dielectric breakdown, associated with anisotropic etch processes above the level of the MIM capacitor.

[0012] A further advantage of the present invention is providing a method of fabricating an MIM capacitor within a multilayer semiconductor device by standard semiconductor fabrication processes that may offer improved yields and enhanced long term reliabiltiy.

[0013] In order to attain the above and other advantages, according to an exemplary embodiment of the present invention, disclosed herein is a multilayer semiconductor device comprising a metal-insulator-metal (MIM) capacitor that includes a first metal plate, a dielectric layer, and a second metal plate, a nitride etchstop layer formed above the MIM capacitor, a first interlayer dielectric formed on top of the nitride etchstop layer, and a first via and a second via that extend through at least the first interlayer dielectric to contact the nitride etchstop layer.

[0014] According to another exemplary embodiment of the present invention, the nitride etchstop layer is deposited directly upon the MIM capacitor.

[0015] According to another exemplary embodiment of the present invention, the first metal plate and the second metal plate correspond to a bottom plate and a top plate of the MIM capacitor, respectively.

[0016] According to another exemplary embodiment of the present invention, the multilayer semiconductor device further comprises a second interlayer dielectric formed between the top plate of the MIM capacitor and the nitride etchstop layer.

[0017] According to another exemplary embodiment of the present invention, the second interlayer dielectric comprises a thickness of about 1500 Ã... to about 10,000 Ã....

[0018] According to another exemplary embodiment of the present invention, the thickness of the nitride etchstop layer is about 500Ã... to about 1500 Ã....

[0019] According to another exemplary embodiment of the present invention, a thickness of the nitride etchstop layer is about 700 Ã... to about 1200 Ã....

[0020] According to another exemplary embodiment of the present invention, the multilayer semiconductor device further comprises a wiring level that is electrically connected to at least one of the first metal plate and the second metal plate.

[0021] According to another exemplary embodiment of the present invention, a method of fabricating a multilayer semiconductor device comprises forming an MIM capacitor that includes a first metal plate, a dielectric layer formed on the first metal plate, and a second metal plate formed on the dielectric layer, patterning the second metal plate, depositing a nitride etchstop layer above the MIM capacitor, forming a first interlayer dielectric on the nitride etchstop layer, forming a first via and a second via through at least the first interlayer dielectric by an anisotropic etch process to contact the nitride etchstop layer above the patterned second metal plate and above the first metal plate, respectively, and removing portions of the nitride etchtop layer, where the first via and the second via contact the nitride etchstop layer.

[0022] According to another exemplary embodiment of the present invention, patterning the second metal plate is accomplished by an anisotropic etch process.

[0023] According to another exemplary embodiment of the present invention, the selective via etch chemistry may include any of the group of argon, nitrogen, C4F8 and argon or oxygen, and carbon monoxide.

[0024] According to another exemplary embodiment of the present invention, the depositing of the nitride etchstop layer is directly upon the MIM capacitor.

[0025] According to another exemplary embodiment of the present invention, the method of fabricating the multilayer semiconductor device further comprises patterning at least one of the first metal plate and the dielectric layer by the

anisotropic etch process.

[0026] According to another exemplary embodiment of the present invention, the method of fabricating a multilayer semiconductor device further comprises patterning a wiring level in electrical contact with at least one of the first metal plate and the second metal plate by an anisotropic etch process.

[0027] According to another exemplary embodiment of the present invention, the method of fabricating the multilayer semiconductor device further comprises forming a second interlayer dielectric between the second metal plate and the nitride etchstop layer.

[0028] According to another exemplary embodiment of the present invention, the method of fabricating a multilayer semiconductor device, including an MIM capacitor, comprises patterning a metal top plate of the MIM capacitor by an anisotropic etch process, depositing a nitride etchstop layer above the MIM capacitor, forming a first interlayer dielectric on the nitride etchstop layer, and forming a first via through the first interlayer dielectric by an anisotropic etch process to contact the nitride etchstop layer.

[0029] According to another exemplary embodiment of the present invention, the method of fabricating the multilayer semiconductor device, including an MIM capacitor, further comprises removing a first portion of the nitride etchstop layer above the MIM capacitor, so that, the first via contacts the metal top plate.

[0030] According to another exemplary embodiment of the present invention, the method of fabricating the multilayer semiconductor device, including an MIM capacitor, further comprises forming a second via through the first interlayer dielectric by an anisotropic etch process to contact the nitride etchstop layer.

[0031] According to another exemplary embodiment of the present invention, the method of fabricating the multilayer semiconductor device, including an MIM capacitor, further comprises removing a second portion of the nitride etchstop layer above the MIM capacitor, so that, the second via contacts a metal bottom plate of the MIM capacitor.

[0032] According to another exemplary embodiment of the present invention, the method of fabricating the multilayer semiconductor device, including an MIM capacitor, further comprises forming a second interlayer dielectric between the metal top plate and the nitride etchstop layer.

[0033] Thus, the present invention overcomes the problems of the conventional methods and structures of an MIM capacitor disposed within a multilayer semiconductor device by using a nitride etchstop film that may prevent either dielectric breakdown of an MIM capacitor, associated with anisotropic etching at levels above the MIM capacitor, or plate-to-plate electrical shorting, caused by etch-through of the top plate. The present invention also enhances the long term reliability of an MIM capacitor, when compared to conventional fabrication methods by depositing an insulating nitride film above the MIM capacitor, which may reduce dielectric degradation caused by excessive electrical charging of the MIM capacitor during anisotropic process above the MIM capacitor.

Brief Description of the Several Views of the Drawings

[0034] The foregoing and other aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawing, in which:

[0035] Figure 1 illustrates a multilayer semiconductor device 100 in an exemplary embodiment of the present invention; and

[0036] Figure 2 illustrates a flowchart of a method for making the multilayer semiconductor device 100 of Figure 1 in an exemplary embodiment of the present invention.

Detailed Description of the Invention

[0037] Generally, the present invention takes advantage of depositing a nitride etchstop layer above an MIM capacitor, which is included in a multilayer semiconductor device, to prevent dielectric degradation of the capacitor dielectric by anisotropic etching processes taking place above the MIM capacitor.

[0038] In various exemplary embodiments, the deposition of the nitride etchstop layer

may occur after patterning the top plate of the MIM capacitor, after patterning the MIM capacitor and a wiring level electrically connected to the MIM capacitor, and after a thin intervening interlayer dielectric is deposited between the patterned top plate and the nitride etchstop layer. The nitride etchstop layer may provide an insulative layer, which may prevent electrical charge from reaching the plates of the MIM capacitor during an anisotropic etch occurring above the MIM capacitor and may also provide a layer upon which an anisotropic etch process is stopped. The dielectric layer of the MIM capacitor may, thus, attain better integrity and the long term reliability of the MIM capacitor may also be enhanced. The nitride etchstop layer may also prevent plate-to-plate electrical shorting by stopping etch-through of the top plate and prevent breakdown of insulative properties of the dielectic.

[0039] Referring to Figure 1, a first metal plate 1 of an MIM capacitor may be formed above a semiconductor substrate of a multilayer semiconductor device 100. The first metal plate 1 may be deposited by, for example, sputtering, plating, polishing, and other metal deposition processes well known in the art. The first metal plate 1 may be electrically connected to a wiring level 9. The first metal plate 1 may be made of aluminum, copper, titanium nitride, tantalum nitride, and other metals and alloys of these metals well known in the art. The first metal plate 1 may have a thickness of about 500 Ã... to about 15,000 Ã... and may have an area of about 0.0001 mm^2 to about 1 mm^2.

[0040] In various exemplary embodiments, the first metal plate 1 may be patterned by conventional etch processes. Further, the first metal plate 1 may form a portion of a metal wiring level 9 and the first metal plate 1 and its corresponding wiring level 9 may both be patterned by, for example, an isotropic etch process.

[0041] A dielectric layer 2 of the MIM capacitor may be formed over the first metal plate 1 by conventional photomasking and deposition processes, for example, chemical vapor deposition (CVD), plasma enhanced CVD, atomic layer CVD, organometallic CVD, and other deposition processes well known in the art. The dielectric layer 2 may be made of silicon oxide, silicon nitride, silicon oxynitride, tantalum pentoxide, aluminum oxide, titanium oxide, and other dielectric materials well known in the art. The dielectric layer 2 may have a thickness of about 50 Ã... to about 1200 Ã....

[0042] A second metal plate 3 of the MIM capacitor is formed above the dielectric layer 2. The second metal plate 3 may be deposited by, for example, sputtering, and other metal deposition processes well known in the art. The second metal plate 3 may be electrically connected to a wiring level 10. The second metal plate 3 may be made of aluminum, copper, titanium nitride, tantalum nitride, and other metals and alloys of these metals well known in the art. The second metal plate 3 may have a thickness of about 500 Ã... to about 5000 Ã... and usually has an area less than that of the first metal plate 1.

[0043] In various exemplary embodiments, the second metal plate 3 may be patterned by an anisotropic etch process, such as, for example, RIE. In various exemplary embodiments, the second metal plate 3 may form a portion of a metal wiring level 10 and the second metal plate 3 and its corresponding wiring level 10 may both be patterned by, for example, an anisotropic etch process.

[0044] A nitride etchstop layer 4 is formed above the MIM capacitor by, for example, plasma enhanced CVD (PECVD), atomic layer CVD, organometallic CVD, or other deposition processes well known in the art. In various exemplary embodiments, the thickness of the nitride etchstop layer may be from about 500 Ã... to about 1500 Ã..., with a preferred thickness of about 700 Ã....

[0045] In various exemplary embodiments, deposition of the nitride etchstop layer 4 may occur, for example, after the second metal plate 3 of the MIM capacitor has been patterned, after the MIM capacitor and an associated wiring level has been patterned, and optionally, after a relatively thin second interlayer dielectric 8 of about 1500 Ã... to about 10,000 Ã... has been deposited on the MIM capacitor, subsequent to the patterning of the MIM capacitor.

[0046] A first interlayer dielectric 5 may be formed above the nitride etchstop layer 4 by, for example, CVD, PECVD, and other dielectric deposition processes well known in the art. The first interlayer dielectric 5 may be made of silicon oxide, fluorinated silicon oxide, SiLK, and other dielectric materials well known in the art. The first interlayer dielectric 5 may have a thickness greater than about 3000 Ã....

[0047] Referring to Fig. 1, a first via 6 may be formed through the first interlayer

dielectric 5 to the nitride etchstop layer 4 above the second metal plate 3 by an anisotropic etch process, such as, for example, RIE. Similarly, in various exemplary embodiments, a second via 7 may be formed through the first interlayer dielectric 5 to the nitride etchstop layer 4 above the first metal plate 1 by an anisotropic etch process.

[0048] Portions of the nitride etchstop layer 4 may be removed (not shown in Fig. 1), where the first via 6 and the second via 7 contact the nitride etchstop layer 4 above the second metal plate 3 and the first metal plate 1, respectively, by a selective via etch chemistry. The selective via etch chemistry may include a wet etch or a reactive ion etch including any of argon, nitrogen, C^4F^8 and argon or oxygen, carbon monoxide, and other via etch chemistries well known in the art, which may remove the nitride etchstop layer without damaging the dielectric layer 2 of the MIM capacitor by either excessive electrical charging or ion/plasma damage.

[0049] Referring to Figure 2, a method of fabricating a multilayer semiconductor device, including an MIM capacitor, includes at least the steps of patterning a metal top plate of the MIM capacitor by an anisotropic etch process 1, depositing a nitride etchstop layer above the MIM capacitor 2, forming a first interlayer dielectric on the nitride etchstop layer 3, and forming a first via through the interlayer dielectric by an anisotropic etch process to contact the nitride etchstop layer.

[0050] Experimental results indicate that an MIM capacitor, within a multilayer semiconductor device 100, on which a nitride etchstop layer is formed after patterning of the MIM capacitor, possesses superior dielectric properties as measured by time dependent dielectric breakdown. The devices are found to have a tighter distribution of lifetimes under high voltage stress more indicative of intrinsic dielectric breakdown.

[0051] The nitride etchstop layer presumably provides a surface above the top plate of the MIM capacitor on which an anisotropic via etch process, for example, RIE, is stopped, thereby, preventing etch-through of the top plate of the MIM capacitor and consequently, plate-to-plate electrical shorting. In addition, that the insulative properties of the nitride etchstop layer presumably prevent excessive electrical charge from reaching the metal plates of the MIM capacitor and consequent dielectric degradation.

[0052] The benefits of providing a dielectric layer of the MIM capacitor, which is not subject to dielectric degradation or plate-to-plate electrical shorting, are improved manufacturing yields and enhanced long term reliability.

[0053] The nitride layer on top of the MIM capacitor provides a chemical etchstop layer for the via RIE to stop on, thereby, widening the process window for the via RIE process. The via RIE overetch can now be a less controlled process while neither incurring the risk of affecting the reliability of the MIM capacitor nor causing etch-through of the top plate nor allowing for too much erosion of the metal level that the via lands on.

[0054] While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

[0055] Further, it is noted that Applicants' intent is to encompass equivalents of all claim elements, even if amended later during prosecution.